

WHAT IS CLAIMED IS:

1. A device, comprising:
 - 5 a voltage level detector comprising an NMOS tail current transistor; and
a voltage generator coupled to a gate of the tail current transistor;
wherein the voltage generator is configured to deliver a voltage to the gate of the
10 tail current transistor;
wherein a first component of the voltage is approximately equal to the threshold
voltage of NMOS transistors comprised in the device; and
15 wherein a second component of the voltage is approximately constant with respect
to variations in operating temperature as well as variations in transistor
fabrication parameters;
 2. The device of claim 1, wherein the voltage generator comprises a diode-connected
20 NMOS transistor and a constant current sink configured to produce the first
component of the voltage;
wherein the source of the diode-connected NMOS transistor is coupled to the
input of a constant current sink;
25 wherein the output of the current sink is coupled to a negative supply;

wherein in the channel geometry of the transistor, W/L , and the current drawn by the current sink, I , are such that $(I/\beta)^{1/2} \ll V_t$, the NMOS threshold voltage;

5 wherein first component of the voltage is produced as the gate-source voltage of the diode-connected NMOS transistor;

3. The device of claim 1, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.
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4. The device of claim 1, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce the sum of the first and second components of the voltage at the gate of the diode-connected NMOS transistor;
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wherein the output of the bandgap voltage reference is coupled to the inverting (negative) input of the amplifier;

20 wherein the source of the diode-connected NMOS transistor is coupled to the non-inverting (positive) input of the amplifier;

wherein the output of the amplifier is coupled to the gate of the PMOS transistor;

25 wherein the drain of the PMOS transistor is coupled to the gate and drain of the diode-connected NMOS transistor; and

wherein the source of the PMOS transistor is coupled to a positive supply.

5. The device of claim 1, wherein the first component of the voltage provides the threshold voltage required to turn on the tail current transistor, despite variations in operating temperature as well as variations in transistor fabrication parameters.
- 5 6. The device of claim 1, wherein the second component of the voltage provides a constant effective voltage, V_{eff} , for the tail current transistor, which produces the tail current, I_t , proportional to beta of the NMOS process according to the relationship: $I_t = (\beta/2) * (V_{eff})^2$.
- 10 7. The device of claim 1, further comprising a differential pair of NMOS transistors whose emitters are coupled to the drain of the tail current transistor and in which the channel width to length ratio of the first transistor differs from that of the second transistor.
- 15 8. The device of claim 1, wherein the trip point of the voltage level detector is approximately constant despite variations in operating temperature as well as variations in transistor fabrication parameters.
9. A device, comprising:
- 20 a differential amplifier comprising an NMOS tail current transistor; and
- a voltage generator coupled to a gate of the tail current transistor;
- 25 wherein the voltage generator is configured to deliver a voltage to the gate of the tail current transistor;
- wherein a first component of the voltage is approximately equal to the threshold voltage of NMOS transistors comprised in the device over variations in

operating temperature as well as variations in transistor fabrication parameters; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature as well as variations in transistor fabrication parameters;

10. The device of claim 9, wherein the voltage generator comprises a diode-connected NMOS transistor and a constant current sink configured to produce the first component of the voltage;

wherein the source of the diode-connected NMOS transistor is coupled to the input of a constant current sink;

- wherein the output of the current sink is coupled to a negative supply;

wherein in the channel geometry of the transistor, W/L , and the current drawn by the current sink, I , are such that $(I/\beta)^{1/2} \ll V_t$, the NMOS threshold voltage;

wherein first component of the voltage is produced as the gate-source voltage of the diode-connected NMOS transistor;

11. The device of claim 9, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.

12. The device of claim 9, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce the sum of the first and

second components of the voltage at the gate of the diode-connected NMOS transistor;

5 wherein the output of the bandgap voltage reference is coupled to the negative
 (inverting) input of the amplifier;

 wherein the source of the diode-connected NMOS transistor is coupled to the
 positive (non-inverting) input of the amplifier;

10 wherein the output of the amplifier is coupled to the gate of the PMOS transistor;

 wherein the drain of the PMOS transistor is coupled to the gate and drain of the
 diode-connected NMOS transistor; and

15 wherein the source of the PMOS transistor is coupled to a positive supply.

13. The device of claim 9, wherein the first component of the voltage provides the
 threshold voltage required to turn on the tail current transistor, despite variations
 in operating temperature as well as variations in transistor fabrication parameters.

20 14. The device of claim 9, wherein the second component of the voltage provides a
 constant effective voltage, V_{eff} , for the tail current transistor, which produces the
 tail current, I_t , proportional to beta of the NMOS process according to the
 relationship: $I_t = (\beta/2) * (V_{eff})^2$.

25 15. The device of claim 9, wherein the offset voltage of the differential amplifier is
 approximately constant despite variations in operating temperature as well as
 variations in transistor fabrication parameters.

16. A method comprising:
- generating a constant reference voltage;
- 5 generating a voltage that approximates the threshold voltage of a NMOS process over variations in operating temperature as well as variations in transistor fabrication parameters; and
- generating a composite voltage that is the sum of the constant reference voltage
- 10 and the voltage that approximates the threshold voltage of the NMOS process.
17. The method of claim 16 further comprising, applying the composite voltage to the gate of a tail current transistor of a voltage level detector.
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18. The method of claim 17, wherein the threshold component of the composite voltage turns on the tail current transistor despite variations in operating temperature as well as variations in transistor fabrication parameters.
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19. The method of claim 18, wherein the constant reference component of the composite voltage produces a tail current for the voltage level detector that is proportional to beta for the NMOS process.
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- 25 The method of claim 19, wherein the trip point of the voltage level detector is approximately constant despite variations in operating temperature as well as variations in transistor fabrication parameters.
21. The method of claim 16 further comprising, applying the composite voltage to the gate of a tail current transistor of a differential amplifier.

22. The method of claim 21, wherein the threshold component of the composite voltage turns on the tail current transistor despite variations in operating temperature as well as variations in transistor fabrication parameters.

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23. The method of claim 22, wherein the constant reference component of the composite voltage produces a tail current for the differential amplifier that is proportional to beta for the NMOS process.

10 24. The method of claim 23, wherein the offset voltage of the differential amplifier is approximately constant despite variations in operating temperature as well as variations in transistor fabrication parameters.

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